



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: RESH-001.....

Inventor(s): Pete Dahl, Byron Dickinson, Margie Levine and Paul Rodman
Serial No.: 09/714,722 Group Art Unit: 2811
Filed: 11/15/00 Examiner: Tran, Thien F.
Title: OPTIMIZATION OF ABUTTED-PIN HIERARCHICAL PHYSICAL DESIGN

Commissioner of Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Information Disclosure Statement Submitted Pursuant to 37 C.F.R. 1.97(b)

The citations referenced herein, copies attached, may be material to the examination of the above-identified application and are, therefore, submitted in compliance with the duty of disclosure as defined in 37 C.F.R. 1.56. The Examiner is requested to make these citations of official record in the application.

This Information Disclosure Statement submitted in accordance with 37 C.F.R. 1.97(b) is not to be construed as a representation that a search has been made, that additional items material to the examination of this application do not exist, or that any one or more of these citations constitute prior art under 35 U.S.C. 102.

The Examiner's attention is respectfully directed to the following U.S. Patents:

<u>Pat. No.</u>	<u>Pat. Title</u>	<u>Grant Date</u>
5,757,658	PROCEDURE AND SYSTEM FOR PLACEMENT OPTIMIZATION OF CELLS WITHIN CIRCUIT BLOCKS BY OPTIMIZING PLACEMENT OF INPUT/OUTPUT PORTS WITHIN AN INTEGRATED CIRCUIT DESIGN	05/26/98
5,309,370	METHOD FOR PLACEMENT OF CONNECTORS USED INTERCONNECTING CIRCUIT COMPONENTS IN AN INTEGRATED CIRCUIT	05/03/94

The Examiner's attention is respectfully directed to the following Foreign Patents:

<u>Pat. No.</u>	<u>Pat. Title</u>	<u>Grant Date</u>
WO 00/67163	PLACEMENT-BASED PIN OPTIMIZATION METHOD AND APPARATUS FOR COMPUTER-AIDED CIRCUIT DESIGN	11/09/00

Please direct all correspondence concerning the above-identified application to the following address:

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Patent Application

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Form 1449**U.S. Patent Documents**

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A	5,757,658	05/26/98	Rodman, et al.	364	491	03/06/96
	B	5,309,370	05/03/94	Wong	364	490	12/13/90
	C						
	D						
	E						
	F						
	G						
	H						
	I						
	J						
	K						

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No
	L	WO00/67163	11/09/00	WIPO	G06F	17/50		
	M							
	N							
	O							
	P							
	Q							

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	R	
	S	
	T	
Examiner		Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered.
Include copy of this form with next communication to applicant.